BridgeX® Firmware fw-BridgeX

Rev 8.5.0000
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1 Introduction

These are the release notes for the BridgeX® gateway firmware, fw-BridgeX Rev 8.5.0000. This firmware supports the following protocols:

- Ethernet over InfiniBand (EoIB)
- Fibre Channel over Ethernet (FCoE)
- Fibre Channel over InfiniBand (FCoIB)
- Ethernet to Ethernet (PHyX®)

After burning the new firmware, reboot your system to activate the new firmware. Failing to do so will result in an error when running the RUN_FW command.

2 Firmware fw-BridgeX Compatibility

Firmware fw-BridgeX Rev 8.5.0000 is compatible with:

- *BridgeX Programmer's Reference Manual (PRM)*, Rev 1.30 or later
- *Mellanox BridgeX Management (BXM)* software version 2.1.1100
3 Changes and New Features

3.1 BridgeX Firmware v8.5.0000

- Added support for "ALL VLAN" vHub
- Increased the buffer size of VL15 to avoid packets’ drops
- Added support for filtering LLDP packets to FabricIT BXM
- Added Shared context table option - 5k vNICs
- Added DCBX support of receiving DCBX packets with a VLAN tag
- Added the ability to send FabricIT BXM Advertisement and Multicast vNIC alive messages
- Added the ability to send packets from external Ethernet ports to FabricIT BXM to enable LACP
- Modified SL2VL mapping to enables changes on the fly
- Added different tx serdes sets for different cables capability
- Added FCoE frame aging
- Added the ability to control external module tx_disable
- Added a verification test to check if the external Phy module exists only in PhyX mode
- Enabled 4th Fibre Channel port in FCoE
- Added bits for clause37 page timer
- Added offset calibration to rx training in Ethernet
- Added the ability to reset to cl37_active and idle_active in clause37 flow upon link failure
- Sent IDLEs and CL37 pages to work with Finisar and Delta modules
- Changed vl_arb_low_cap vl_arb_high_cap in port info mad
- Added the ability to compare application tlv in DCBX
- Added Fibre Channel counters: frames lost, r_rduys lost
- Added clause37 flow fix - Added phy_type indication for int port in devide internal pib, flow checked sgmii linkup, and for int side
- Added anti spoofing changes

3.2 BridgeX Firmware v8.4.0000

- Added DCBX support
- Added support for new LED management control in GT boards and in SGMII on internal ports.
- Added new port counters (FC fsm state change, eth_rx_giant)
- Added Query Device Temperature command interface (PHYX_GET_TEMPERATURE)
• Added support for setting internal port attributes from the BridgeX Manager using SET_PORT and QUERY_PORT mailboxes
• Added eth_mtu_current field to QUERY_PORT mailbox
• Enabled IRISC
• Added support for reading Fibre Channel speeds from SFP module (upon raising Fibre Channel link)
• Added tuning serdes parameters on different boards
• Separated the PHYX_SET_PORT_GROUP attributes between KR and force XFI per port
• Added the capability to retrieve current Fibre Channel TX_credit & RX_credit
• Added INI control for the advertise abilities of the AN page
• Added configuring number of Tx and Rx options
• Added Fibre Channel RX adaptation variable to INI
• Added INI option to properly close i2c by firmware before the software resets

3.3 BridgeX Firmware v8.3.3160

BridgeX firmware v8.3.3160 does not contain any new changes/features.

3.4 BridgeX Firmware v8.3.3000

• Added VL separation support
• Added PhyX® command interface
• Added ARP proxy lookup mode
• Added anti-spoofing support for multicast Packets
• Added RSS configuration
• Made Ethernet link change events configurable
• Added Ethernet link change events support in managed PhyX® mode
• Added link policy reflection in PhyX® mode
• Added module rate select configuration in Fibre Channel port (access by i2c or GPIO).
• Added external port module state change
• Added port drop counters
• Added counters per priority port
• Added support to XFI detection in the parallel detect.
• Added reset counters policy
• Added MTU configuration
• The chips are now presented as 2 port IB with a single node_guid
4 Tested Cables and Modules in Rev 8.5.0000

The following are the cables and modules tested in this release:

**Table 1 - Tested Cables and Modules**

<table>
<thead>
<tr>
<th>Length</th>
<th>Connector</th>
<th>Ordering Part</th>
<th>Cable Type</th>
<th>Media</th>
<th>Max Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>1M</td>
<td>QSFP</td>
<td>MC2206130-001</td>
<td>Passive</td>
<td>Copper</td>
<td>QDR/FDR10</td>
</tr>
<tr>
<td>5M</td>
<td>QSFP</td>
<td>MC2206128-005</td>
<td>Passive</td>
<td>Copper</td>
<td>QDR/FDR10</td>
</tr>
<tr>
<td>10M</td>
<td>QSFP</td>
<td>MC2206230-010</td>
<td>Active</td>
<td>Copper</td>
<td>IB QDR</td>
</tr>
<tr>
<td>15M</td>
<td>QSFP</td>
<td>MFS4R12CB-015</td>
<td>Active</td>
<td>Fiber</td>
<td>IB QDR</td>
</tr>
<tr>
<td>30M</td>
<td>QSFP</td>
<td>MC2206310-030</td>
<td>Active</td>
<td>Fiber</td>
<td>IB QDR</td>
</tr>
<tr>
<td>3M</td>
<td>SFP+</td>
<td>MC3309130-003</td>
<td>Passive</td>
<td>Copper</td>
<td>10GigE</td>
</tr>
<tr>
<td>Module</td>
<td>SFP+</td>
<td>MFM1T02A-LR</td>
<td>Active</td>
<td>Optical Module</td>
<td>10GigE</td>
</tr>
<tr>
<td>Module</td>
<td>SFP+</td>
<td>MFM1T02A-SR</td>
<td>Active</td>
<td>Optical Module</td>
<td>10GigE</td>
</tr>
</tbody>
</table>
## 5 Bug Fixes

### Table 2 - Bug Fixes

<table>
<thead>
<tr>
<th>Index</th>
<th>Issue</th>
<th>Description</th>
<th>Found in FW Version</th>
<th>Fixed in FW Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Fixed Fibre Channel RX</td>
<td>Fixed an issue with the Fibre Channel RX adaptation flow.</td>
<td>8.4.0000</td>
<td>8.5.0000</td>
</tr>
<tr>
<td>2.</td>
<td>Software reset flow</td>
<td>Fixed an issue with the software reset flow.</td>
<td>8.4.0000</td>
<td>8.5.0000</td>
</tr>
<tr>
<td>3.</td>
<td>TrapRepress</td>
<td>Fixed an issue with the TrapRepress.</td>
<td>8.4.0000</td>
<td>8.5.0000</td>
</tr>
<tr>
<td>4.</td>
<td>LID configuration</td>
<td>LID configuration caused FCoIB to fail in LIDs higher than 0x0080.</td>
<td>8.3.3160</td>
<td>8.4.0000</td>
</tr>
<tr>
<td>5.</td>
<td>Fibre Channel link status in EXT PROPERTIES interface</td>
<td>The link status report showed the link as down when it was up.</td>
<td>8.3.3160</td>
<td>8.4.0000</td>
</tr>
<tr>
<td>6.</td>
<td>PhyX link reflection</td>
<td>PhyX link reflection did not work when ports were connected back to back.</td>
<td>8.3.3160</td>
<td>8.4.0000</td>
</tr>
<tr>
<td>7.</td>
<td>Fragmented errors</td>
<td>Fixed an issue with the inter-packet gap in PhyX. Added ini to control ipg 4/8.</td>
<td>8.3.3160</td>
<td>8.4.0000</td>
</tr>
<tr>
<td>8.</td>
<td>PCI timeout</td>
<td>PCI response was too long thus resulting in PCI timeout.</td>
<td>8.3.3160</td>
<td>8.4.0000</td>
</tr>
<tr>
<td>9.</td>
<td>Fibre Channel credits</td>
<td>Credit leakage issues.</td>
<td>8.3.3160</td>
<td>8.4.0000</td>
</tr>
<tr>
<td>10.</td>
<td>eth configuration issues</td>
<td>Fixed PhyX issues related to the PhyX mode.</td>
<td>8.3.3160</td>
<td>8.4.0000</td>
</tr>
<tr>
<td>11.</td>
<td>Auto negotiation</td>
<td>Occasionally in the InfiniBand auto negotiation, the DDR setup was raised in SDR.</td>
<td>8.3.3160</td>
<td>8.4.0000</td>
</tr>
<tr>
<td>12.</td>
<td>Cable removal</td>
<td>The links stopped going up after a series of cable plug-ins and unplug-ins.</td>
<td>8.3.3160</td>
<td>8.4.0000</td>
</tr>
</tbody>
</table>